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(54) IMAGE/VOICE COMPRESSION DEVICE AND SEMICONDUCTOR INTEGRATED CIRCUIT FOR IMAGE/VOICE COMPRESSION

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the number of chips and the number of parts in the whole AV equipment and to reduce the size and weight of the AV equipment by arranging a compression means for compressing image or voice informationa means for extending compressed information and a communication means for communicating with the external of the device on the same semiconductor substrate.
SOLUTION: A video signal outputted from a camera part 101 is inputted to a memory 103 through a memory controller 102 built in a CODEC LSI 100. The information is returned to the CODEC LSI 100 again and compressed by a compression processing circuit 104 and then the compressed information is inputted to an MPU 107 through a system bus 106. In the case of receiving time informationthe information is inputted to the memory 103 through the system bus 106 and the memory controller 102returned to the CODEC LSI 100 through the controller 102 and decoded by an extension processing circuit 105. The memory controllers 102110 are driven by clock pulses generated from an oscillator 103 connected to the CODEC LSI 100.

CLAIMS

[Claim(s)]
[Claim 1]A function to perform compression or extension of a picture thru/or speech information.
A function which can communicate a compressed picture thru/or speech information with the device exterior.
A means of communication for communication with a compression means which is the picture speech compression device provided with the aboveand performs compression of said picture thru/or speech informationan extension means which elongates condensed information compressed by said compression meansand said device exterior was constituted on the same semiconductor substrate.

[Claim 2]An integrated circuit constituting a means of communication for communication with a compression means which performs compression of a picture thru/or speech informationan extension means which elongates condensed information compressed by said compression meansand said device exterior on the same semiconductor substrate.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the device which has an image compression functionand relates to an image compression device with the function which changes into a bit stream the picture information compressed especiallyand outputs it.
[0002]
[Description of the Prior Art]The picture information compression extension device (an encoder/decoder) based on standardssuch as H.261 of ITU_T adviceMPEG Iand IIis generally spreading by progress of image compression technology and LSI technology.
[0003]In these picture information compression extension devicealthough CODEC and signal-processing LSI for it are generally called CODEC_LSIsmall low-pricing of CODEC_LSI is promoted as one of the key devices of multimedia.
[0004]The information compressed by CODEC is considered [storing in storage mediasuch as an optical discor being transmitted and used using an ISDN circuitan ATM communication networketc. in the form of the bit stream of the compressed dataand]. For this reasonat ITU_Tthe regulation about accumulation thru/or transmission is given by H.221 adviceone etc. copy of MPEG II adviceetc.and especially the latter is explained by 480 to TV academic journal Vol.49 No.5(April'95 item)pp489 Yoshimura etc. "a system."
[0005]
[Problem(s) to be Solved by the Invention]When the above-mentioned CODEC is built in AV equipmentsuch as a camera and VTRit is natural to perform

processingssuch as exchange of the video audio information etc. which were being conventionally performed by transmission and reception of the analog signaland movementby bit stream communication of condensed information.
[0006]Thereforein the AV device which has a CODEC function. It is desirable to output the compressed video information to other CODEC apparatus together with the compression extension function of picture informationor to give a communication function so that extension reproduction of the image sound information can be carried out from the bit stream conversely inputted from other CODEC apparatus.
[0007]By the waythe bit stream used for communication between such devicesExcept for information required for CODEC processing of image sound information as shown in the conventional example by the kind of transmission linereliabilitya topologyetc.For examplethe address information of a transmitting end and a receiving endetc. are added and transmitted in most casesand though naturalwith information required for CODEC processingthese dissociate and must be managed. Thereforethe CODEC apparatus with a communication function with the device exterior is (1) CODEC portion. Portion which carries out the generation interpretation of the bit stream outputted and inputted by (2) devices (3) Communication portion which outputs and inputs a actual bit stream Although three portions are requiredEach portion of these and consideration very sufficient [for a small weight saving] for them in which especially (1) is independently constituted by (2) and (3) were not made conventionally.
[0008]
[Means for Solving the Problem]A memory and a memory controller which are used for the above-mentioned CODEC devicei.e.CODEC_LSI built in thisfor orthogonal transformation of image dataetc. are indispensable. A communication function also performs real time communication in the bit rate of a bit stream generated by CODECand the different bit rateorSimilarly from a reason of making it correspond to a jitter generated in a transmission line by a certain cause etc.a memory and a memory controller are neededand each is realized by same semiconductor process.
[0009]Soa means of communication for communication with a compression means which performs compression of a picture thru/or speech informationan extension means which elongates condensed information compressed by a compression meansand the device exterior consisted of this inventions on the same semiconductor substrate. ThereforeCODEC_LSI does not need to form separately a memory for compression extensionmemories for communicationand those controllersit reduces and the small weight saving of a chip number of the whole AV equipmentsuch as a camera and VTRand the number of parts which built in CODEC can be carried out.
[0010]
[Embodiment of the Invention]Drawing 1 is used for below and one example of this invention is described to it. This example explains the example which gave the transmitting function of the serial signal to the image compression device.

[0011]Firstusing the figures (a)picture information is compressed and the process in which condensed information is transmitted to the device exterior is explained.
[0012]The video signal outputted from the camera part 101 is inputted into the memory chip 103 via the memory controller 102 constituted by CODEC_LSI100 (A). After this information is again returned to CODEC_LSI at suitable time and being encoded in (B) and the compression processing circuit 104 (compression)it is inputted into MPU106 via the system bath 105 (C). In adding information required for record of recording time etc.for examplestoring in the recording medium 107 in MPUin recording thisand transmitting (D) and thisFor examplefixed length's communication packet is generatedand after adding processing of carrying out division insertion of the encode signal to the data divisiona signal is returned to CODEC_LSI via a system bath (E). In CODEC_LSIafter carrying out the Para Thilly conversion with the Para Thilly converter 112 in which this was provided by the communications department 109it outputs via FIFO memory 111 controlled by the memory controller 110.
[0013]The process in which uses the figure (b) nextreceive the compressed picture informationand this is elongated (decoding) is explained.
[0014]After inputting by FIFO buffer 111 converselyThilly para conversion of the case of reception is carried outand it is inputted into MPU via a system bath (F). If it is the receipt information which MPU interpreted this input signalfor exampleincluded compressed image signal informationAfter inputting the portion in connection with this into the memory chip 103 via a system bath and a memory controller (H)similarly it is returned to CODEC_LSI to suitable timing via a memory controllerand is decoded in (I) and the expansion process circuit 105.
[0015]Although each memory controller 102 and 110 constituted by CODEC_LSI performs control of a memory chipand control of the FIFO memory for communication by the above processingBoth drive by the clock pulse generated from the radiator 103 connected to CODEC_LSI.
[0016]Since CODEC_LSI does not need to provide the memory for communicationand its controller and others separately and it is not necessary to install an independent radiator if it does in this wayThe chip number of the whole AV equipmentsuch as a camera and VTRand the number of parts which built in CODEC can be reducedand a small weight saving can be attained.
[0017]Although the FIFO memory for communication is constituted from this example in CODEC_LSI as mentioned above and the memory for compression processing is considered as another chipIt is what took into consideration that the memory for compression processing needed a megger bit order to the thing the thing of the scale of a kilo bit order of this composition may generally be sufficient as whose FIFO memory for communicationThough naturalconstituting both on CODEC_LSI by future near improvement in an LSI degree of location is also considered.
[0018]When high-speed transmission of the bit stream information packet-ized especially is carried outInserting and transmitting error detection informationincluding a CRC (Cyclic Redunduncy Check) bit etc.to the final position

of a packet is generally performedand the circuit for it may be given to the communications department of CODEC_LSI. For examplea CRC error detection circuit is realizable in an easy returned type shift register and a logical sum (Exclusive Or) circuit as generally known.

[0019]Drawing 2 is used above and one another example of this invention is described to it. With the figurepicture information is compressed and the process in which condensed information is transmitted to the device exterior is explained.

[0020]In this exampleit is an example which uses a part of address of the memory chip connected to CODEC_LSI for compressionand uses other portions for communication.

[0021]Although the example which constitutes the FIFO memory for communication on CODEC_LSI in said example was describedin this examplewith CODEC_LSIa certain portion on the address of the memory of another chip is used for compression extensionand other portions are used for communication.

[0022]Although the video signal outputted from the camera part 201 is inputted into the memory chip 203 via the memory controller 202 constituted by CODEC_LSI200The address area X for compression extension is beforehand established in the memory chip hereand an input is performed in this area (A). This information is again returned to CODEC_LSI at suitable timeand (B) and after being encoded (compression)it is inputted into MPU207 via the system bath 206. In adding information required for record of recording time etc.for examplestoring in the recording medium 208 in MPUin recording thisand transmitting thisFor examplefixed length's communication packet is generatedand after adding processing of carrying out division insertion of the encode signal to the data divisiona signal is again returned to CODEC_LSI via a system bath. At CODEC_LSIafter writing in the address area Y for communication which is not in agreement with the area for compression extension where the signal was again provided in the memory chip 203 beforehand via the memory controller 202it reads on frequency suitable for communication.

[0023]Other one example of this invention is shown in drawing 3. The video interface circuit where drawing 3 shows the example of 1 concrete composition of CODEC_LSIand 301 outputs and inputs a signal to a cameraand 302310Buffer RAM which performs signal input and output of each blockthe decision circuit where 303 judge intra of P and B pictureand inter304 A DCT/IDCT (Discrete Cosine Transform/ Inverese Discrete CosineTransform = discrete cosine transform / reverse discrete cosine transform) processing circuitThe quantization inverse quantizing circuit where 305 performs quantizationinverse quantizationand rate control that keeps a generated code amount constantThe VLC/VLD circuit where 306 performs variable length coding and decryptionTG circuit where 307 generates the control pulses of the operation timing of each blockThe control circuit of external RAM and 309 308 The detector circuit of a motion vectorThe data register in which 311 controls the interface circuit of an audio signal312 controls the communication interface circuit of compressed dataand 313 controls the operational mode of each blocketc.and 314 are interface circuits with external

MPU. By the above compositionit corresponds to the graphical data compression and extension which use DCT transformationvariable length codingand bidirectional motion compensation inter frame predictioni.e.MPEGand a JPEG standard by this CODEC_LSI. Hereaftereach mode is explained along the flow chart of drawing 5 thru/or drawing 14.

[0024]1. JPEG compression mode (1)

In drawing 5the JPEG compression mode of the video signal inputted from the camera is explained. Firstthe video signal inputted from the camera is inputted from the video interface circuit 301and is transmitted to external RAM315 by the external RAM control circuit 308. Nextthe external RAM control circuit 308 reads a video signal from external RAM315changes a video signal into a block type from a raster styleand memorizes it to buffer RAM302. The video signal of buffer RAM302 is changed into a DCT coefficient by the DCT/IDCT circuit 304It is quantized by the quantization inverse quantizing circuit 305 for every DC (direct current) ingredient and AC (exchange) ingredientand variable length coding is performed by the VLC/VLD circuit 306and it is returned to buffer RAM302. In this waythe obtained compressed data is memorized by external RAM315 and outputted to an MPU bus by the external RAM control circuit 308 through the MPU interface circuit 306.

[0025]2. Explain the extension mode of the JPEG compression data obtained from the MPU bus in JPEG extension mode drawing 6. Firstafter the compressed data inputted from the MPU bus via the MPU interface circuit 306 is transmitted to external RAM315 by the external RAM control circuit 308it is memorized by buffer RAM302. Variable-length decryption by the VLC/VLD circuit 306inverse quantization by the quantization inverse quantizing circuit 305and IDCT conversion by the DCT/IDCT circuit 304 are performedand the compressed data memorized by buffer RAM302 is returned to buffer RAM302. In this waythe elongated video signal is sent to external RAM315 by the external RAM control circuit 308It is changed into raster data from block data by the external RAM control circuit 308and is outputted as a video signal through the video interface circuit 301.

[0026]3. JPEG compression mode (2)

In drawing 7JPEG compression of the video signal is carried out from an MPU busand the processing again returned to an MPU bus is explained. The video signal inputted from the MPU interface circuit 306 is transmitted to external RAM315 by the external RAM control circuit 308. Nextthe external RAM control circuit 308 reads a video signal from external RAM315and memorizes it to buffer RAM302. The video signal of buffer RAM302 is changed into a DCT coefficient by the DCT/IDCT circuit 304It is quantized by the quantization inverse quantizing circuit 305 for every DC (direct current) ingredient and AC (exchange) ingredientand variable length coding is performed by the VLC/VLD circuit 306and it is returned to buffer RAM302. In this waythe obtained compressed data is memorized by external RAM315 and outputted to an MPU bus by the external RAM control circuit 308 through the MPU interface circuit 306.

[0027]4. Explain the processing at the time of carrying out image display of the

video signal from an MPU bus as it is in image display mode drawing 8. the video signal data inputted via the MPU interface circuit 306 -- the external RAM control circuit 308 -- external RAM315 -- it is transmitted. The external RAM control circuit 308 reads this signalperforms conversion to raster data from block dataand is outputted as a video signal via the video interface circuit 301.
[0028]According to this example of operationafter inputting and compressing a video signal from MPUvia the video interface circuit 301it can come out as it is and can draw without outputting or compressing compressed data into MPU again.
[0029]5. Explain compression processing of I picture in MPEG compressed mode in MPEG compression (1) I picture drawing 9. Firstthe video signal inputted from the camera is inputted from the video interface circuit 301and is transmitted to external RAM315 by the external RAM control circuit 308. Nextthe external RAM control circuit 308 reads a video signal from external RAM315changes a video signal into a block type from a raster styleand memorizes it to buffer RAM302. The video signal of buffer RAM302 is changed into a DCT coefficient by the DCT/IDCT circuit 304It is quantized by the quantization inverse quantizing circuit 305 for every DC (direct current) ingredient and AC (exchange) ingredientand variable length coding is performed by the VLC/VLD circuit 306and it is returned to buffer RAM302. In this waythe obtained compressed data is memorized by external RAM315 and outputted to an MPU bus by the external RAM control circuit 308 through the MPU interface circuit 306. The processing so far is the same as that of the case of JPEG compression.
[0030]On the other handthe data in which quantization was performed by the quantization inverse quantizing circuit 305Inverse quantization is carried out by the quantization inverse quantizing circuit 305buffer RAM302 memorizeswhen IDCT conversion is carried out by the DCT/IDCT circuit 304it is elongatedand the external RAM control circuit 308 memorizes as a recon SUTORAKUTO picture external RAM315. This recon SUTORAKUTO picture will be used for the compression processing of P picture and B picture described later.
[0031](2) Explain compression processing of I picture in MPEG compressed mode in P picture drawing 10. The video signal inputted from the camera is inputted from the video interface circuit 301and is transmitted to external RAM315 by the external RAM control circuit 308. Nextthe external RAM control circuit 308 reads a video signal from external RAM315changes a video signal into a block type from a raster styleand memorizes it to buffer RAM302. The processing so far is the same as that of the case of I picture.
[0032]On the other handthe MV (motion vector) detector circuit 309 compares the data of a recon SUTORAKUTO picture previously explained to be the data by which raster block conversion was carried outand obtains MV (motion vector) value which shows such correlation.
[0033]The external RAM control circuit 308 reads the block data of the recon SUTORAKUTO picture shown with this MV value from external RAM315and memorizes it to buffer RAM302 as prediction image data.
[0034]The decision circuit 302 judges whether which processing of intr which

compresses only by its own pictureor inter using the correlation of the picture of order is performed from the picture image data obtained in this wayMV valueand prediction image dataor Half Pel compensation is performed. And DCT transformation by the DCT/IDCT circuit 304 and quantization by the quantization inverse quantizing circuit 305 are performed.

[0035]The video signal of buffer RAM302 is changed into a DCT coefficient by the DCT/IDCT circuit 304It is quantized by the quantization inverse quantizing circuit 305 for every DC (direct current) ingredient and AC (exchange) ingredientand variable length coding is performed by the VLC/VLD circuit 306and it is returned to buffer RAM302. In this waythe obtained compressed data is memorized by external RAM315 and outputted to an MPU bus by the external RAM control circuit 308 through the MPU interface circuit 306.

[0036]The data in which quantization was performed by the quantization inverse quantizing circuit 305 on the other handInverse quantization is carried out by the quantization inverse quantizing circuit 305buffer RAM302 memorizeswhen IDCT conversion is carried out by the DCT/IDCT circuit 304it is elongatedand the external RAM control circuit 308 memorizes as a recon SUTORAKUTO picture external RAM315. This recon SUTORAKUTO picture will be used for compression processing of B picture described later.

[0037](3) Explain compression processing of I picture in MPEG compressed mode in B picture drawing 11. The video signal inputted from the camera is inputted from the video interface circuit 301and is transmitted to external RAM315 by the external RAM control circuit 308. Nextthe external RAM control circuit 308 reads a video signal from external RAM315changes a video signal into a block type from a raster styleand memorizes it to buffer RAM302. The processing so far is the same as that of the case of I picture.

[0038]On the other handthe MV (motion vector) detector circuit 309The data of the recon SUTORAKUTO picture of I previously explained to be the data by which raster block conversion was carried outor P picture is comparedand MV which shows the correlation of MV (motion vector) value and the recon SUTORAKUTO picture of the future which show correlation with the past recon SUTORAKUTO picture is obtained.

[0039]The external RAM control circuit 308 reads the block data of the recon SUTORAKUTO picture of two sheets shown with this 2 ** MV value from external RAM315and memorizes it to buffer RAM302 as prediction image data.

[0040]The decision circuit 302 from the picture image dataMV valueand prediction image data which were obtained in this way. . [whether which processing of intra which compresses only by its own pictureor inter using the correlation of the picture of order is performedand] In interit is judged whether judgment in the prediction mode whether to use the estimated image of whether the estimated image of the future is usedusing the past estimated imagethe pastor the futureand Half Pel compensation are performed. And DCT transformation by the DCT/IDCT circuit 304 and quantization by the quantization inverse quantizing circuit 305 are performed.

[0041]The video signal of buffer RAM302 is changed into a DCT coefficient by the DCT/IDCT circuit 304It is quantized by the quantization inverse quantizing circuit 305 for every DC (direct current) ingredient and AC (exchange) ingredientand variable length coding is performed by the VLC/VLD circuit 306and it is returned to buffer RAM302. In this waythe obtained compressed data is memorized by external RAM315 and outputted to an MPU bus by the external RAM control circuit 308 through the MPU interface circuit 306. This procedure is the same as that of the case of P picture.
[0042]6. Explain the elongation processing of I picture in MPEG extension mode in MPEG extension (1) I picture drawing 12. Firstafter the compressed data inputted from the MPU bus via the MPU interface circuit 306 is transmitted to external RAM315 by the external RAM control circuit 308it is memorized by buffer RAM302. Variable-length decryption by the VLC/VLD circuit 306inverse quantization by the quantization inverse quantizing circuit 305and IDCT conversion by the DCT/IDCT circuit 304 are performedand the compressed data memorized by buffer RAM302 is returned to buffer RAM302. In this waythe elongated video signal is sent to external RAM315 by the external RAM control circuit 308It is changed into raster data from block data by the external RAM control circuit 308and is outputted as a video signal through the video interface circuit 301. Fixed time maintenance of the image data of external RAM315 is carried out for DECODE of P and B picture.
[0043](2) Explain the elongation processing of P picture in MPEG extension mode in P picture drawing 13. Firstafter the compressed data inputted from the MPU bus via the MPU interface circuit 306 is transmitted to external RAM315 by the external RAM control circuit 308it is memorized by buffer RAM302. Variable-length decryption according [the compressed data memorized by buffer RAM302] to the VLC/VLD circuit 306inverse quantization by the quantization inverse quantizing circuit 305and IDCT conversion by the DCT/IDCT circuit 304 are performed. The procedure so far is the same as that of the case of I picture.
[0044]By MV value and intra/inter which were obtained from the data by which variable-length decryption was carried out in the VLC/VLD circuit 306 on the other handthe external RAM control circuit 308I picture or P picture preceded from external RAM315 is read for recon SUTORAKUTOand it memorizes to buffer RAM302 as prediction data.
[0045]The decision circuit 303 performs an intra/inter judging etc. from the data and prediction image data by which IDCT conversion was carried outrestores extension dataand memorizes it to buffer RAM302. In this waythe elongated video signal is sent to external RAM315 by the external RAM control circuit 308It is changed into raster data from block data by the external RAM control circuit 308and is outputted as a video signal through the video interface circuit 301. Fixed time maintenance of the image data of external RAM315 is carried out for DECODE of P and B picture.
[0046](3) Explain the elongation processing of B picture in MPEG extension mode in B picture drawing 14. Firstafter the compressed data inputted from the MPU bus via the MPU interface circuit 306 is transmitted to external RAM315 by the

external RAM control circuit 308it is memorized by buffer RAM302. Variable-length decryption according [the compressed data memorized by buffer RAM302] to the VLC/VLD circuit 306inverse quantization by the quantization inverse quantizing circuit 305and IDCT conversion by the DCT/IDCT circuit 304 are performed. The procedure so far is the same as that of the case of I picture.

[0047]With MV value obtained from the data by which variable-length decryption was carried out in the VLC/VLD circuit 306 on the other handintra/interand prediction modethe external RAM control circuit 308I and P which get mixed up from external RAM315and B picture are read for recon SUTORAKUTOand it memorizes to buffer RAM302 as prediction data.

[0048]The decision circuit 303 performs an intra/inter judging etc. from the data and prediction image data by which IDCT conversion was carried outrestores extension dataand memorizes it to buffer RAM302. In this waythe elongated video signal is sent to external RAM315 by the external RAM control circuit 308It is changed into raster data from block data by the external RAM control circuit 308and is outputted as a video signal through the video interface circuit 301.

[0049]As mentioned aboveaccording to this compositionit can elongate by changing and compressing MPEG and JPEG. Although MPEG compression of the video signal was carried out from the MPU bus and explanation was omitted about the processing again returned to an MPU busit cannot be overemphasized that it is realizable by processing adapting the case of JPEG.

[0050]Nextin this compositionthe timing in the case of performing compression of MPEG1 standard and extension operation is explained using drawing 4. Drawing 4 (a) is the timing in compressionand this figure shows the cycle M= 3 of GOP size N= 6Iand P picture as an example. When compressing the video signal of NTSC at 30 Hz nowsince the frame rate of NTSC is 60 Hzsince the signal of one of the two's field is unnecessaryit is not incorporated into CODEC_LSI. Thusthe incorporated frame rate 30Hz video signal is processed as it explained [above-mentioned]and it carries out real-time compression at 1 frame period. Drawing 4 (b) is a figure showing the timing of extension operation. Since unlike compression operations the extension operation does not need to perform MV detection and does not need to perform DCT and IDCT continuouslya compressive half grade is enough as processing time. As shown in this figure1 field-period extension operation is carried outand the next 1 field period can realize real-time extension by stopping extension operation. If it is made to output the signal of the same frame over 2 field periodsthe elongated video signal can be outputted as a 60-Hz signaland also when displaying by NTSCit will not have the necessity for a special frame rate convertereither. Drawing 4 (c) is a figure showing other examples of the timing of extension operation. As shown in this figureif it is made to perform ** field period extension operationdouble-speed reproduction can carry out easily.

[0051]Drawing 15 is a figure showing the layout of CODEC-LSI of this invention. "m_b_t" 1501 is a processing circuit which constitutes a part of external RAM control circuit 308mr_j1502 is a processing circuit which constitutes the part and the decision circuit 303 of the external RAM control circuit 3081503 is a

processing circuit which constitutes the MPU interface circuit 306c_r1504 is a processing circuit which constitutes the quantization inverse quantizing circuit 305the interface circuit 311 of an audio signalthe communication interface circuit 312 of compressed dataand the interface circuit 314 with external MPUe_a1505 is a processing circuit which constitutes a part of video interface circuit 301 and detector circuit 309 of a motion vector1506 is a processing circuit which constitutes a part of detector circuit 309 of a motion vector1507 is a processing circuit which constitutes a DCT/IDCT processing circuitand 1508 is a processing circuit which constitutes the quantization inverse quantizing circuit 305.

[0052]"mcra1" 1511mcra21512mcra31513and "mcra3" 1514 are RAM circuits which constitute buffer RAM302cahram41515 and 1521 are RAM circuits which constitute buffer RAM310r_ram1516 and 1523 are the RAM circuits for quantization inverse quantizing circuitserams11517erams11518and "erams1" 1519 are the RAM circuits for detector circuit 309 of a motion vector1520 is a RAM circuit for control circuit 308 of external RAMand 1522 is a RAM circuit for DCT/IDCT processing circuit 304.

[0053]As explained aboveCODEC_LSI which can perform 2X reproduction can be realized by easy circuitrywithout according to this examplehaving a special memory etc.since compression and an expansion circuit are constituted in the same semiconductor chip. It cannot be overemphasized that it is realizable by easy circuitry without having a special memory etc. like the above in extension operationwhen performing special reproductionsuch as reverse reproductionsince the half grade at the time of compression operations is enough as the capacity of external RAM.

[0054]

[Effect of the Invention]According to this inventionCODEC_LSI does not need to form separately the memory for compression extensionthe memories for communicationand those controllersand the small weight saving of the chip number of the whole AV equipmentsuch as a camera and VTRand the number of parts which built in CODEC can be reduced and carried out.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]The block diagram of the graphical-data-compression extending apparatus of one example of this invention.

[Drawing 2]The block diagram of the graphical-data-compression extending apparatus of one another example of this invention.

[Drawing 3]The block diagram showing one example of CODEC-LSI of this invention.

[Drawing 4]The figure showing the example of 1 operation of CODEC-LSI of this invention.

[Drawing 5]The figure showing the flow of operation of the JPEG compression of

this invention.
[Drawing 6]The figure showing the flow of operation of JPEG extension of this invention.
[Drawing 7]The figure showing the flow of operation of the JPEG compression of this invention.
[Drawing 8]The figure showing the flow of operation of the image display of this invention.
[Drawing 9]The figure showing the flow of operation of compression of I picture in MPEG of this invention.
[Drawing 10]The figure showing the flow of operation of compression of P picture in MPEG of this invention.
[Drawing 11]The figure showing the flow of operation of compression of B picture in MPEG of this invention.
[Drawing 12]The figure showing the flow of operation of extension of I picture in MPEG of this invention.
[Drawing 13]The figure showing the flow of operation of extension of P picture in MPEG of this invention.
[Drawing 14]The figure showing the flow of operation of extension of B picture in MPEG of this invention.
[Drawing 15]The figure showing the layout of CODEC-LSI of this invention.
[Description of Notations]
100 -- CODEC-LSI
101 -- Camera part
102 -- Memory controller
103 -- Memory
104 -- Compression processing circuit
105 -- Expansion process circuit
106 -- System bath
107 -- MPU
108 -- Storage medium
109 -- Communications department
110 -- Memory controller
111 -- FIFO memory
112 -- The Para Thilly converter
113 -- Radiator.